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(71) Applicant (for all designated States except US): **UNIVERSITY OF KENT** [GB/GB]; The Registry, University of Kent, Canterbury, Kent CT2 7NZ (GB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **MCDONALD-MAIER, Klaus, Dieter** [DE/GB]; 80 Gladstone

Road, Deal, Kent CT14 7ET (GB). **HOPKINS, Andrew, Brian, Thomas** [GB/GB]; Crossings Field, Woodland Road, Lyming, Folkestone, Kent CT18 8ET (GB).

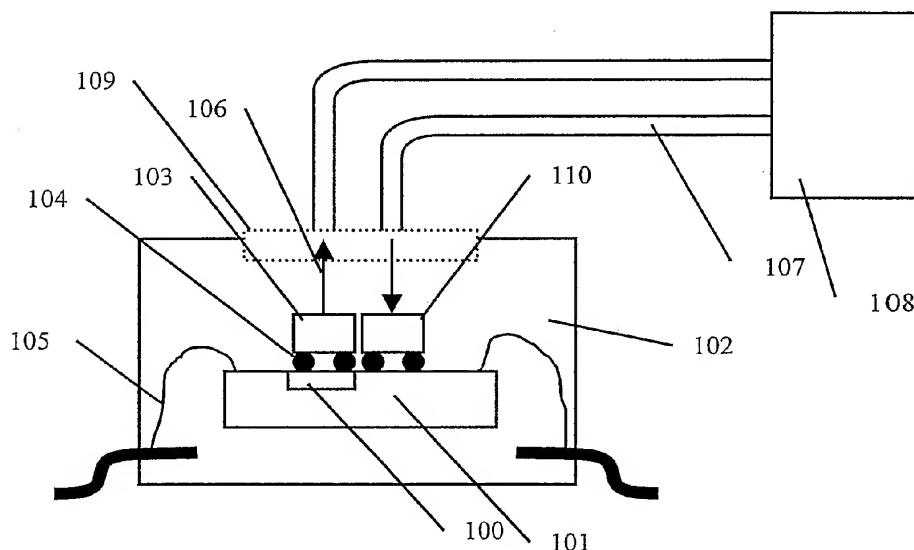
(74) Agent: **ELKINGTON AND FIFE LLP**; Prospect House, 8 Pembroke Road, Sevenoaks, Kent TN13 1XR (GB).

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(54) Title: INTEGRATED CIRCUIT WITH DEBUG SUPPORT INTERFACE



(57) Abstract: A high speed debug support interface has circuits to interface on-chip debug support circuits to a high bandwidth communications port means located on the surface of a system integrated circuit (101) and to on-chip debug support circuits (100). The communication port means can be realised by bonding or integrating special sender and or receiver cells preferably optical sender cells (103) and or optical receiver cells (110) onto the surface of the system integrated circuit (101). The high speed debug support interface communicates with on-chip or in-assembly debug support circuits and an external development tool (108) to permit hardware and software related debugging and development activities, including program tracing, data tracing and memory substitution. The high speed debug support interface has circuits to interface on-chip debug support circuits to system resources such as memory located within the device assembly (102) and connected by the system interconnect.



SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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